CLAIMS

What is claimed is:

1. A method of forming an integrated circuit transistor structure, comprising the steps of:

a) forming a patterned polysilicon layer, and a masking layer thereover, over a gate dielectric over a silicon body;

b) implanting an initial dose of first-conductivity-type dopants to form source/drain extension diffusions in said body;

c) implanting an additional dose of first-conductivity-type dopants, with a deeper stopping distance than said implanting step b), to form main source/drain diffusions in said body;

d) depositing metal overall, and reacting said metal to form a conductive silicide compound in at least some locations; and

e) removing said masking layer after said step b), and before said step c);

wherein said step c), but not said step b), is performed with sidewall spacers present on said patterned polysilicon layer;

and wherein said source/drain diffusions, said source/drain extension diffusions, and a portion of said body under said polycrystalline layer form a transistor;

whereby said step e) reduces the surface dopant concentration of said polysilicon before said step d), and thereby improves the sheet resistance value and/or uniformity after said step d).

2. The method of Claim 1, wherein said masking material is silicon nitride.

3. The method of Claim 1, wherein said sidewall spacers consist predominantly of silicon dioxide.

4. The method of Claim 1, wherein said patterned polysilicon layer is separated from said semiconductor by a gate oxide layer.

5. A method of forming an integrated circuit transistor structure, comprising the steps of:

a) forming a patterned polycrystalline semiconductor layer, and a masking layer thereover, over a semiconductor body;

b) implanting an initial dose of first-conductivity-type dopants to form source/drain extension diffusions in said body;

c) implanting an additional dose of first-conductivity-type dopants to form main source/drain diffusions in said body;

d) depositing metal overall, and reacting said metal to form a conductive metal-semiconductor compound in locations where said metal is deposited on said semiconductor; and

e) removing said masking layer after said step b), and before said step c);

wherein said source/drain diffusions, said source/drain extension diffusions, and a portion of said body under said polycrystalline layer form a transistor;

whereby said step e) improves the sheet resistance value and/or uniformity after said step d)..

6. The method of Claim 5, wherein said sidewall spacers consist predominantly of silicon dioxide.

7. The method of Claim 5, wherein said semiconductor is silicon, and said masking material is silicon nitride.

8. The method of Claim 5, wherein said patterned polycrystalline layer is separated from said semiconductor by a gate dielectric layer.

9. A method of forming an integrated circuit transistor structure, comprising the steps of:

a) forming a patterned polysilicon layer, and a masking layer thereover, over a gate dielectric over a silicon body;

b) implanting an initial dose of first-conductivity-type dopants to form source/drain extension diffusions in said body;

c) implanting an additional dose of first-conductivity-type dopants to form main source/drain diffusions in said body;

d) depositing metal overall, and reacting said metal to form a conductive silicide compound in at least some locations; and

e) removing said masking layer after said step b), and before said step d);

wherein said source/drain diffusions, said source/drain extension diffusions, and a portion of said body under said polycrystalline layer form a transistor;

whereby said step e) reduces the surface dopant concentration of said polysilicon before said step d), and thereby improves the sheet resistance value and/or uniformity after said step d).

10. The method of Claim 10, wherein said masking material is silicon nitride.

11. The method of Claim 10, wherein said sidewall spacers consist predominantly of silicon dioxide.

12. The method of Claim 10, wherein said patterned polysilicon layer is separated from said semiconductor by a gate oxide layer.